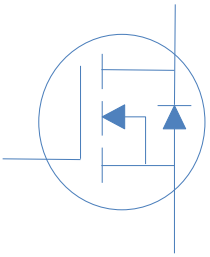
120V N-Ch Power MOSFET

V_{DS}		120	V
$R_{DS(on),typ}$	V_{GS}=10V	9.8	m
$R_{DS(on),typ}$	V_{GS}=4.5V	12.0	m
$I_{D\ (Sillicon\ Limited)}$		36	A



Part Number	Package	Marking
HGA130N12SL	TO-220F	GA130N12SL

Absolute Maximum Ratings at T_J=25℃ (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	T_C=25℃	36	A
		T_C=100℃	25	
Drain to Source Voltage	V_{DS}	-	120	V
Gate to Source Voltage	V_{GS}	-	±20	V
Pulsed Drain Current	I_{DM}	-	180	A
Avalanche Energy, Single Pulse	E_{AS}	L=0.4mH, T_C=25℃	320	mJ
Power Dissipation	P_D	T_C=25℃	38	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to175	℃

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Ambient	R_{JA}	60	℃/W
Thermal Resistance Junction-Case	R_{JC}	4	℃/W

Drain to Source on Resistance	$R_{DS(on)}$	V_{GS}=4.5V, I_D=20A	-	12	17	m
Output Capacitance				222	-	
Total Gate Charge	Q_g(10V)		-	31	-	
Gate to Source Charge	Q_{gs}	V_{DD}=60V, I_D=20A, V_{GS}=10V	-	8	-	nC
Gate to Drain (Miller) Charge	Q_{gd}		-	4	-	
Turn on Delay Time	$t_{d(on)}$		-	11	-	
Rise time	t_r	V_{DD}=60V, I_D=20A, V_{GS}=10V,	-	9	-	ns
Turn off Delay Time	$t_{d(off)}$	R_G=10 ,	-	18	-	
Fall Time	t_f		-	10	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_F=20A	-	0.9	1.2	V
Reverse Recovery Time	t_{rr}	V_R=60V, I_F=20A, dI_F/dt=100A/ s	-	50	-	ns
Reverse Recovery Charge	Q_{rr}		-	75	-	nC

Fig 1. Typical Output Characteristics

Figure 2. On-Resistance vs. Gate-Source Voltage

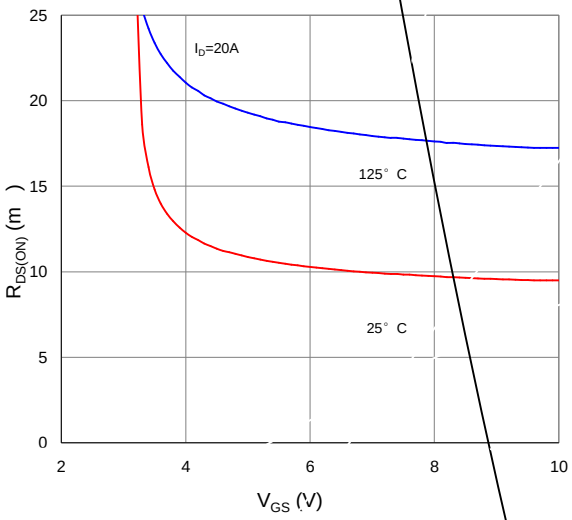


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

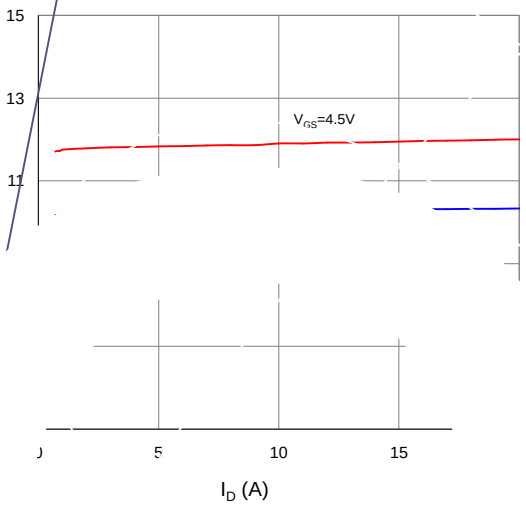
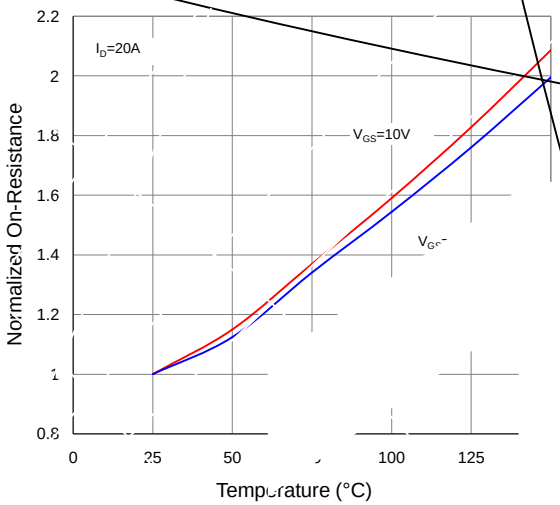
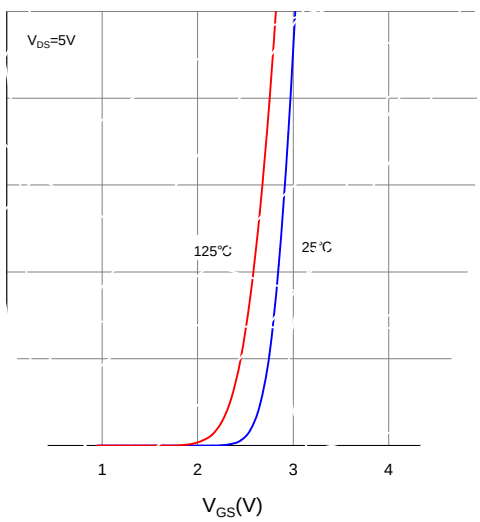


Figure 4. Normalized On-Resistance vs. Junction Temperature



Figu Typical Transfer Characteristics



6. Typical Source-Drain Diode Forward Voltage

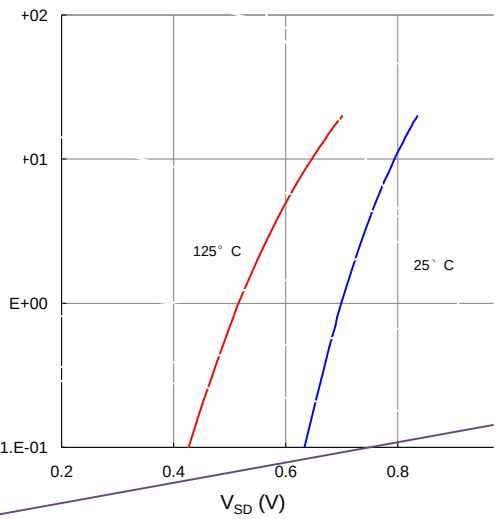


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

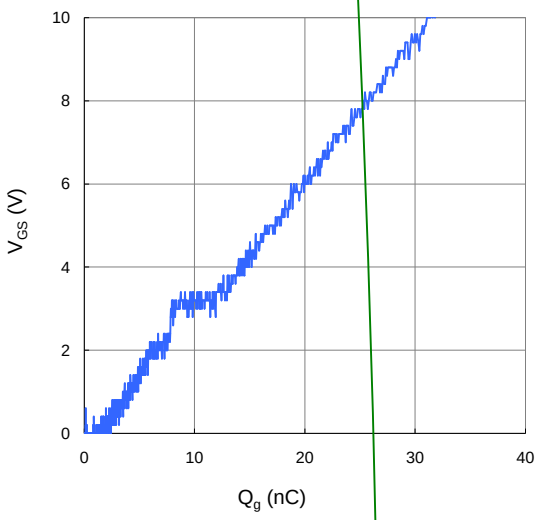


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

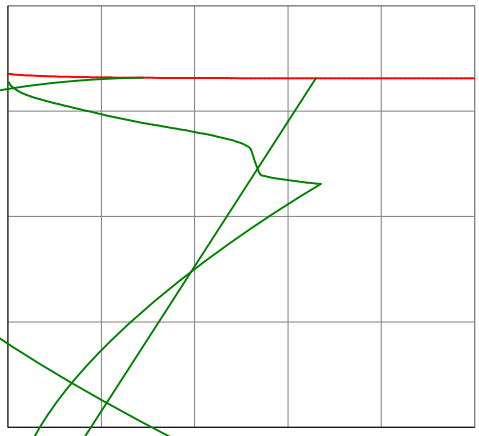
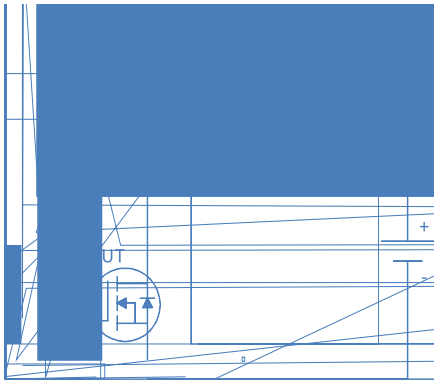


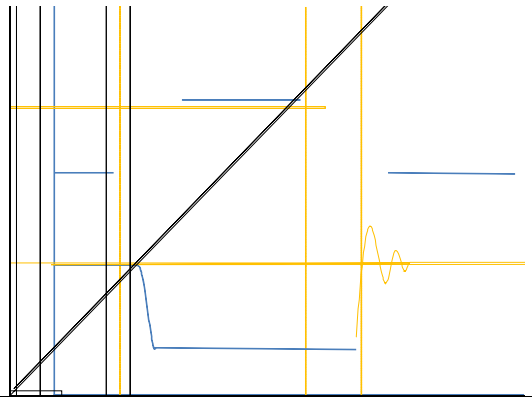
Figure 9. Maximum Safe Operating Area

Figure 10. Maximun Drain Current vs. Case Temperature

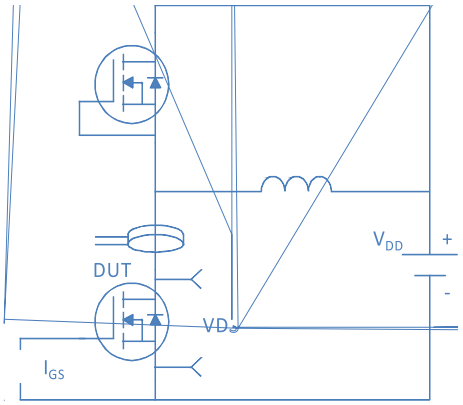
Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient

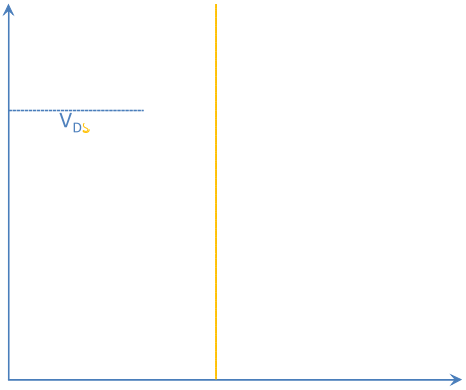
Inductive switching Test



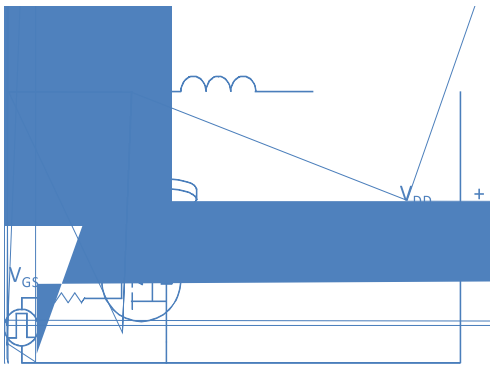


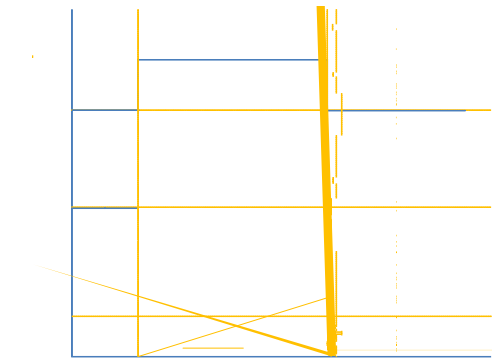
Gate Charge Test



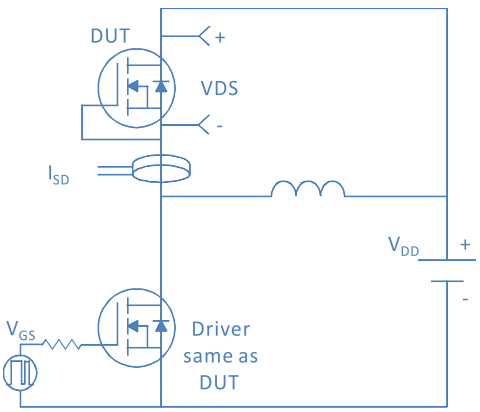


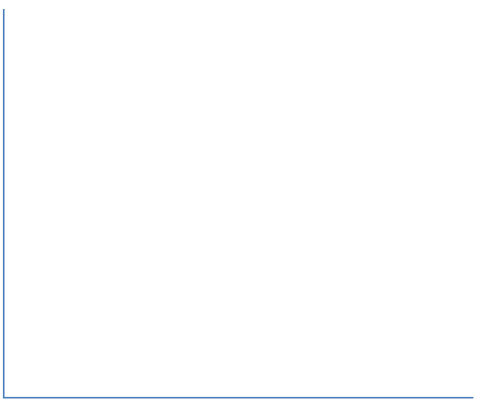
Uclamped Inductive Switching (UIS) Test





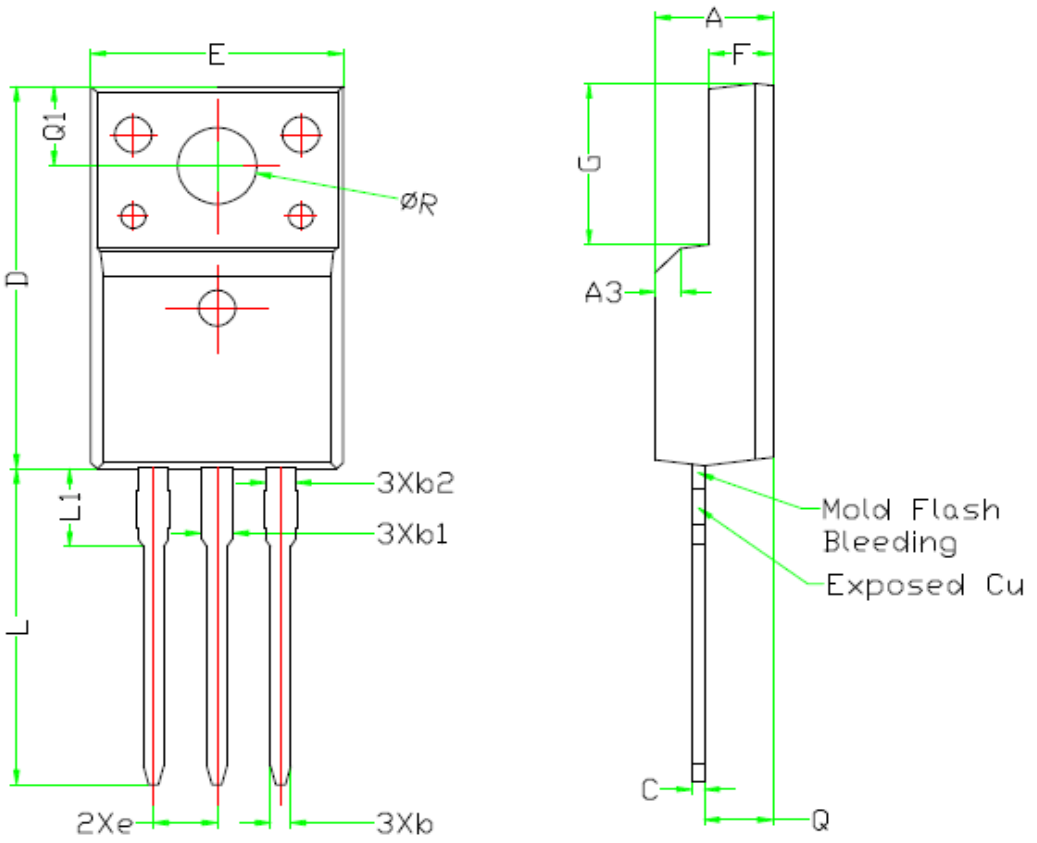
Diode Recovery Test

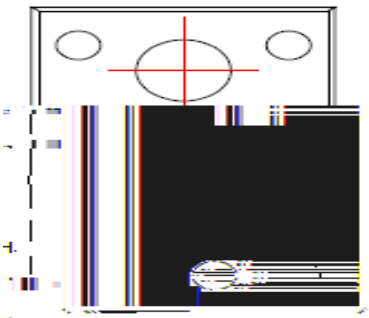




Package Outline

TO-220F, 3 Leads





SYMBOL	DIMENSIONS		
	Min.	Nom.	Max.
A	4.60	4.70	4.80
b	0.77	0.89	0.91
b1	1.20	1.27	1.47
b2	1.20	1.23	1.30
C	0.45	0.50	0.63
D	15.80	15.87	15.97
e		2.54	
E	10.00	10.10	10.30
F	2.44	2.54	2.64
S	6.50	6.70	6.90
L	12.90	13.10	13.20
L1	3.12	3.25	3.38
Q	3.05	3.15	3.25

BOTTOM VIEW

Note:

1. All Dimension Are In mm.

2. Package Body Sizes Exclude Mold Flash And B